LMP92018

LMP92018 Analog System Monitor and Controller

Literature Number: SNAS514A

LMP92018

Analog System Monitor and Controller

1.0 General Description

LMP92018 is a complete analog monitoring and control circuit which integrates an eight channel 10-bit Analog-to-Digital Converter (ADC), four 10-bit Digital-to-Analog Converters (DACs), an internal reference, an internal temperature sensor, a12-bit GPIO port, and a 10MHz SPI interface.

The eight channels of the ADC can be used to monitor rail voltages, current sense amplifier outputs, health monitors or sensors while the four DACs can be used to control PA (Power Amplifier) bias points, control actuators, potentiometers, etc.

Both the ADC and DACs can use either the internal 2.5V reference or an external reference independently allowing for flexibility in system design.

The built-in digital temperature sensor enables accurate (±2.5°C) local temperature measurement whose value is captured in the user accessible register.

The LMP92018 also includes a 12-bit GPIO port which allows for the resources of the microcontroller to be further extended, thus providing even more flexibility and reducing the number of signal interfacing to the microcontroller.

Both the GPIO port and the SPI compatible interface have independent supply pins enabling the LMP92018 to interface with low voltage microcontrollers.

The LMP92018 is available in a space saving 6mm x 6mm LLP 36-pin package and is specified over the full -30°C to +85°C temperature range.

2.0 Features

8 Analog Voltage Monitoring Channels

- 10-bit ADC with programmable input MUX
- Internal/External Reference
- Tolerates high-source impedance at lower sampling rates

4 Programmable Analog Voltage Outputs

- Four 10-bit DACs
- Internal/External Reference
- Drives loads up to 1nF

Voltage Reference

- User-selectable source: external or internal
- Internal Reference 2.5V

Temperature Sensor

- ±2.5°C Accuracy

12-bit GPIO Port

- Each bit individually programmable
- User-selectable rail

SPI-Compatible Bus

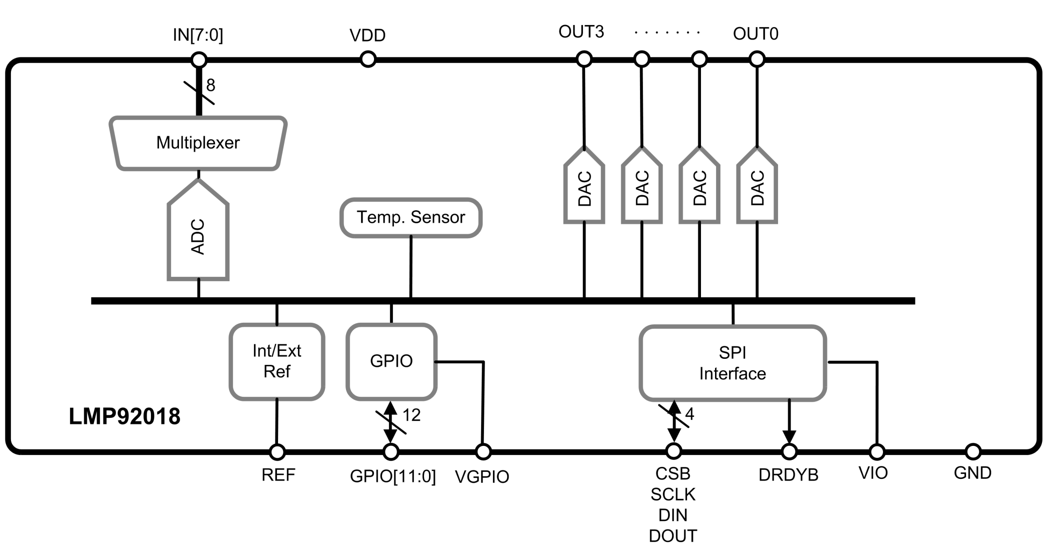
- User-selectable rail

LLP-36 package (6mm x 6mm, 0.5 mm pitch)

3.0 Applications

- Communication Infrastructure
- System Monitoring and Control
- Industrial Monitoring and Control

4.0 Block Diagram



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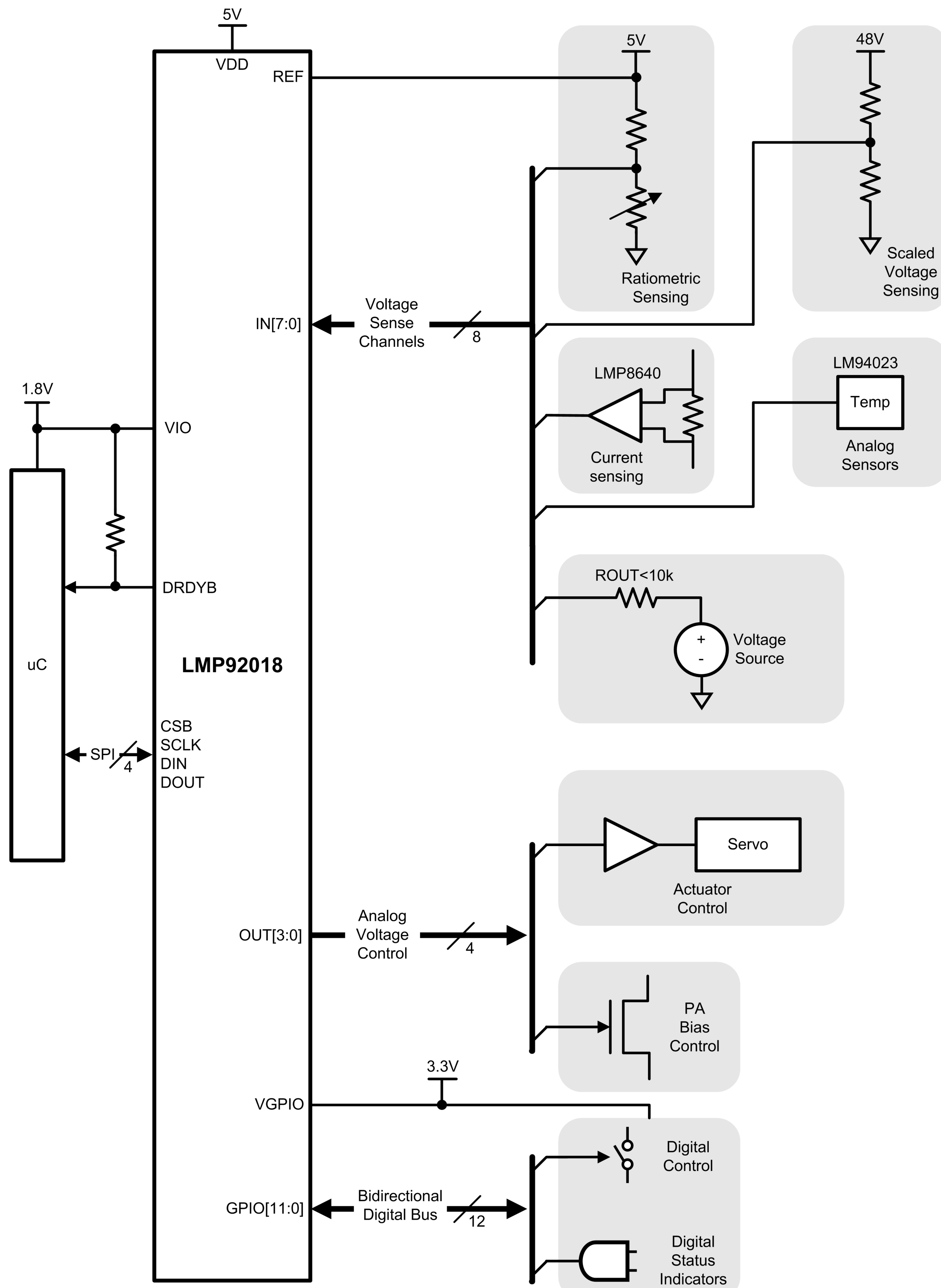
5.0 Typical Application



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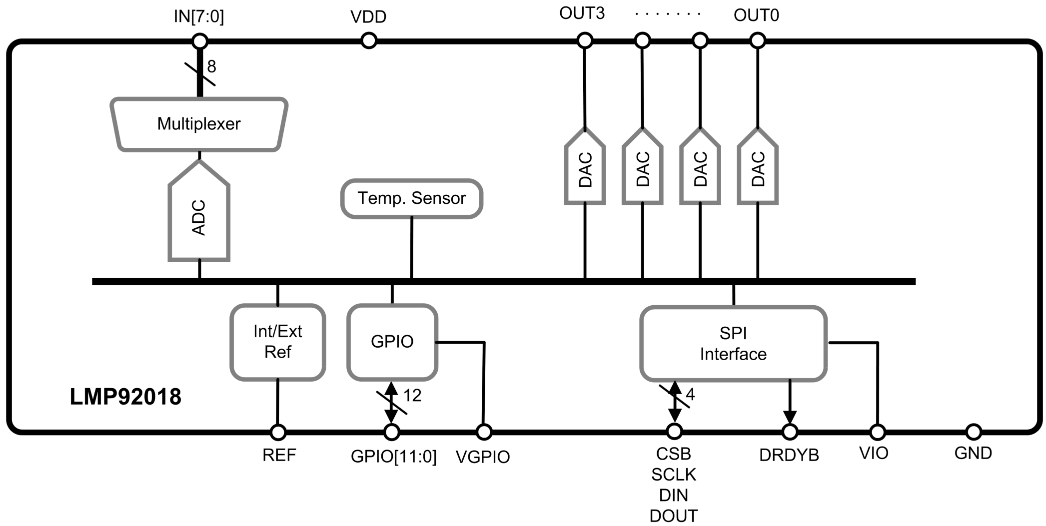

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6.0 Overview

The LMP92018 has a flexible, feature-rich functionality which makes it ideally suited for many analog monitoring and control applications, for example, base-station PA subsystems. This device provides the analog interface between a programmable supervisor, such as a microcontroller, and an analog system whose behavior is to be monitored and controlled by the supervisor.

To facilitate the analog monitoring functionality, the device contains a single 10-bit ADC preceded by a 8-input multiplexor.

The analog control functionality is served by four 10-bit voltage output DACs.

Additional digital monitoring and control can be realized via the General Purpose I/O port GPIO[11:0].

Two more blocks are present for added functionality: a local temperature sensor and an internal reference voltage generator.

6.1 8-CHANNEL ANALOG SENSE WITH 10-BIT ADC

The user can monitor up to 8 external voltages with the 10-bit ADC and its 8-channel input MUX. Typically these voltages will be generated by the analog sensors, instrumentation amplifiers, current sense amplifiers, or simply resistive dividers if high potentials need to be measured.

6.2 PROGRAMMABLE ANALOG CONTROL VOLTAGE OUTPUTS

Four identical individually programmable 10-bit DAC blocks are available to generate analog voltages, which can be used to control bias conditions of external circuits, position of servos, etc.

6.3 INTERNAL DIGITAL TEMPERATURE SENSOR

An on-board digital temperature sensor is available to report the device's own temperature. The temperature sensor output is stored in the internal register for user readback via the SPI interface.

6.4 INTERNAL VOLTAGE REFERENCE SOURCE

The user can choose to enable the internal reference of 2.5V to use with the ADC and/or DACs. The internal reference source can also drive an external load.

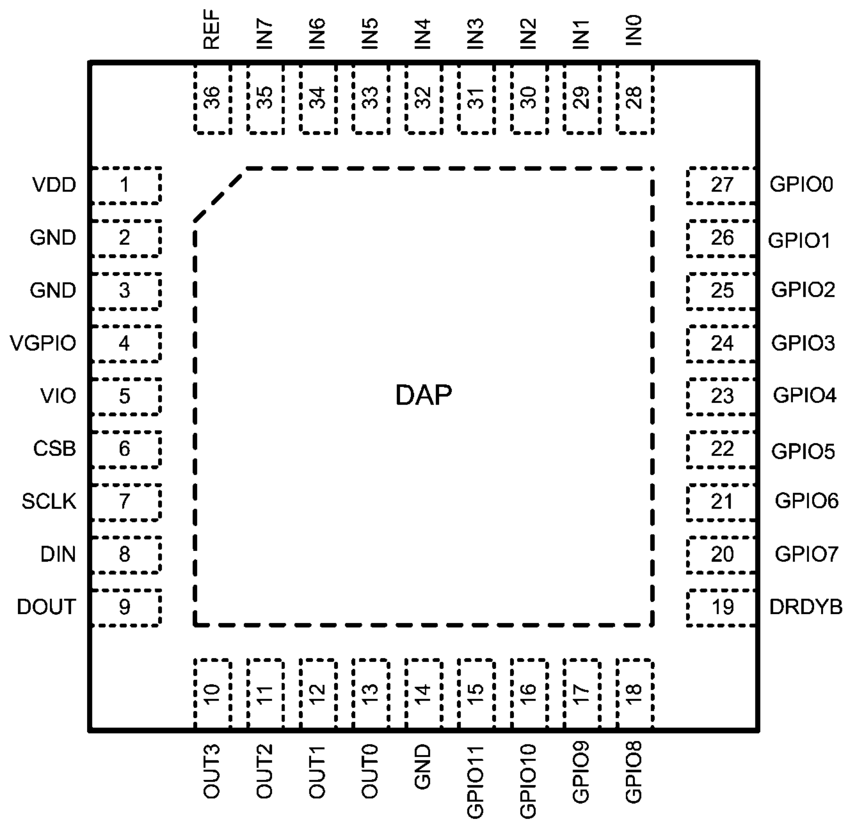
6.5 12-BIT GENERAL PURPOSE I/O

The GPIO port can be used to expand the microcontroller capabilities. This port is memory mapped to the internal register, which in turn is accessible via the SPI interface. Each bit is individually programmable as an input or an output

6.6 SPI INTERFACE

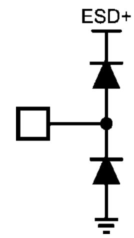
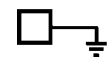
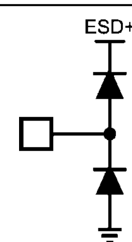
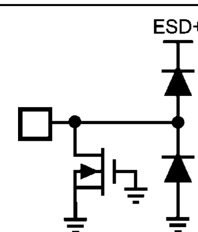
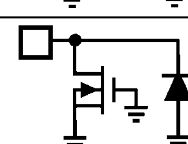
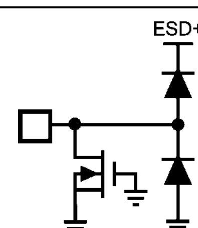
The microcontroller communicates with LMP92018 via a popular SPI interface. This interface provides the user full access to all Data, Status and Control registers of the device.

7.0 Connection Diagram



36–Pin LLP36 (SQA36A)
Top View

8.0 Pin Descriptions

Name	Pin	Function	ESD Structures
VDD	1	Supply rail	
VGPIO	4	GPIO rail	
VIO	5	SPI rail	
GND	2, 3 14	Device Ground	
DAP	*	Die Attach Pad. For best thermal conductivity and best noise immunity DAP should be soldered to the PCB pad which is connected directly to circuit common node (GND).	
IN[7:0]	35:28	Analog input	
OUT[3:0]	10:13	Analog output	
DOUT	9	SPI Data Output	
GPIO[11:0]	15:18; 20:27	General Purpose Digital I/O. Logic level is referenced to VGPIO pin.	
CSB	6	SPI Chip Select, Active LO	
SCLK	7	SPI Data Clock	
DIN	8	SPI Data Input	
DRBYB	19	Data Ready, open-drain active LO	
REF	36	ADC/DAC Voltage Reference Input or Output	

9.0 Ordering Information

Order Number	NS Package Number	Transport Media
LMP92018CISQ	SQA36A	Tape-and reel: 1000 pieces
LMP92018CISQX		Tape-and reel: 2500 pieces

Table of Contents

10.0 Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

VDD Relative to GND	−0.3V to 6.0V
VIO Relative to GND	−0.3V to VDD
VGPIO Relative to GND	−0.3V to VDD
Voltage between any 2 pins (Note 3)	6.0V
Current in or out of any pin (Note 3)	5mA
Current through VDD	32mA, T_A = 125°C 44mA, T_A = 85°C
Current through VGPIO	20mA, T_A = 125°C
Current through GND	54mA, T_A = 125°C 66mA, T_A = 85°C
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
ESD Susceptibility(Note 4)	
Human Body Model	2500V
Machine Model	200V
Charged Device Model	1500V

11.0 Operating Conditions (Note 1, Note 2)

Operating Ambient Temperature	−40°C to 125°C
VDD Voltage Range	4.75V to 5.25V
VIO Voltage Range	1.8V to VDD
VGPIO Voltage Range	1.8V to VDD
DAC Output Load C	0nF to 1nF
θ_{JA}	25.2°C/W
θ_{JC}	2.4°C/W

For Soldering specifications:
See product folder at www.national.com and www.national.com/ms/MS-SOLDERING.pdf.

12.0 Electrical Characteristics

Unless otherwise noted, these specifications apply for VDD=4.75V to 5.25V, REF=VDD, T_A=25°C. **Boldface** limits are over the temperature range of −30°C ≤ T_A ≤ 85°C unless otherwise noted. DAC input code range 12 to 1012. DAC output C_L = 200 pF unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ADC CHARACTERISTICS						
	Resolution with No Missing Codes		**10**		**10**	Bits
DNL	Differential Non-Linearity		**−0.9**		**+1**	LSB
INL	Integral Non-Linearity		**−1**		**1**	LSB
OE	Offset Error		**−2**		**+2**	LSB
OEDRIFT	Offset Error Temperature Drift			0.001		LSB/°C
OEMTCH	Offset Error Match (Note 9)		**−1**		**1**	LSB
GE	Gain Error		**−2**		**2**	LSB
GEDRIFT	Gain Error Temperature Drift			0.001		LSB/°C
GEMTCH	Gain Error Match (Note 9)		**−1**		**1**	LSB
SINAD	Signal-to-Noise Ratio	10 kHz Sine Wave	**58**			dB
THD	Total Harmonic Distortion	10 kHz Sine Wave, up to 5th harmonic	**−69**			dB
SFDR	Spurious Free Dynamic Range	10 kHz Sine Wave	**70**			dBc
PSRR	Power Supply Rejection Ratio	Offset Error change with VDD		−150		dB
		Gain Error change with VDD		−150		dB
DAC CHARACTERISTICS						
	Resolution		**10**		**10**	Bits
	Monotonicity		**10**			Bits
DNL	Differential Non-Linearity	R_L = 100k	**−0.5**		**+0.5**	LSB
INL	Integral Non-Linearity	R_L = 100k	**−2**		**+2**	LSB
OE	Offset Error(Note 6)	R_L = 100k			**10**	mV
OEDRIFT	Offset Error Temperature Drift	R_L = 100k		1		µV/°C
FSE	Full-Scale Error	VDD = 5.25V, REF=5, R_L = 100k, CODE=3FFh	**-0.4**		**+0.3**	%FS
GE	Gain Error(Note 7)	R_L = 100k	**−0.2**		**+0.2**	%FS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
GEDRIFT	Gain Error Temperature Drift	R_L = 100k		1.4		ppm/° C
ZCO	Zero Code Output	I_{OUT} = 200 µA		7		mV
		I_{OUT} = 1mA		31		
FSO	Full Scale Output at code 3FFh	I_{OUT} = 200 µA	**4.975**			V
		I_{OUT} = 1mA	**4.975**			
		R_L = 100k	**4.975**			
I_{OS}	Output Short Circuit Current (Source) (*Note 5*)	VDD = 5V, OUT = 0V, Input Code =3 FFh		–67		mA
I_{OS}	Output Short Circuit Current (Sink) (*Note 5*)	VDD = 5V, OUT = DREF, Input Code = 000h		76		
I_O	Continuous Output Current per Channel (to prevent damage)	T_A = 85° C			**10**	
		T_A = 125° C			**6.5**	
C_L	Maximum Load Capacitance	R_L = 2k or ∞		1000		pF
R_{OUT}	DC Output Impedance	Enabled		1.7		Ω
		Disabled		>20		MΩ
ANALOG INPUT CHARACTERISTICS						
V_{IN}	FS Input Range				**REF**	V
I_{LEAK}	ADC in HOLD or Power Down		**–1**		**+1**	µA
C_{INA}	Input Capacitance	In Acquisition mode		33		pF
		In Conversion mode		3		
REFERENCE CHARACTERISTICS						
	ADC Reference Input Range		**2.5**		**VDD**	V
	DAC Reference Input Range		**2.5**		**VDD**	
	DAC Reference Input Resistance			50		kΩ
	DAC Reference Input Current				**125**	µA
$I_{VREF(ADC)}$	ADC Reference Current, during conversion, average value	External Reference, REF = VDD			**1**	µA
$I_{VREF(PD)}$	REF pin Current in Powerdown				**10**	µA
	REF Output Voltage			2.5		V
	Internal Reference Tolerance		**–0.15**		**0.15**	%
	REF Output Temperature Drift			17		ppm/°C
	REF Output Maximum Current			1		mA
	REF Output Load Regulation				**–0.6**	%
	REF Output Rail Regulation	4.75V≤VDD≤5.25V		±0.04		%
TEMPERATURE SENSOR						
	Resolution			**0.0625**		°C
	Temperature Error (*Note 9*)	–40°C to +125°C	**–2.5**		**+2.5**	°C
DIGITAL INPUT CHARACTERISTICS (GPIO[11:0])						
V_{IH}	Input HIGH Voltage		**0.7x VGPIO**			V
V_{IL}	Input LO Voltage				**0.3x VGPIO**	
	Hysteresis			250		mV
I_{IND}	Digital Input Current			±0.005	**±1**	µA
C_{IND}	Input Capacitance			4		pF
DIGITAL INPUT CHARACTERISTICS (CSB, DIN, SCLK)						
V_{IH}	Input HIGH Voltage		**0.7 x VIO**			V
V_{IL}	Input LO Voltage				**0.3 x VIO**	V
	Hysteresis			250		mV
I_{IND}	Digital Input Current			±0.005	**±1**	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IND}	Input Capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS (GPIO[11:0])						
V_{OL}	Output LO Voltage	I_{OUT} = 200 µA		0.01	**0.4**	V
		I_{OUT} = 1.6 mA VGPIO = VDD = 5V		0.07	**0.4**	
V_{OH}	Output HI Voltage	I_{OUT} = 200µA	**VGPIO-0.2**			V
		I_{OUT} = 1.6 mA VGPIO = VDD = 5V	**VGPIO-0.5**			
IOZH, IOZL	TRI-STATE Output Leakage Current	VGPIO=VDD			**±5**	µA
C_{OUT}	Output Capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS (DOUT)						
V_{OL}	Output LO Voltage	I_{OUT} = 200 µA		0.01	**0.4**	V
		I_{OUT} = 1.6 mA VIO = 3.3V		0.07	**0.6**	V
V_{OH}	Output HI Voltage	I_{OUT} = 200 µA	**VIO-0.2**			V
		I_{OUT} = 1.6 mA VIO = 3.3V	**VIO-0.5**			
IOZH, IOZL	TRI-STATE Output Leakage Current	VGPIO = 1.8V =VDD			**±5**	µA
C_{OUT}	Output Capacitance			4		pF
DIGITAL OUTPUT CHARACTERISTICS (DRDYB)						
V_{OH_MAX}	Maximum Output HI Voltage	I_{OUT} = 1.6 mA VIO = 3.3V to VDD	**VIO-0.5**			µA
V_{OL}	Output LO Voltage	Force 0V or VDD		0.01		V
POWER SUPPLY CHARACTERISTICS						
V_{DD}	Supply Voltage Range		**4.75**	5	**5.5**	V
V_{GPIO}	GPIO Rail Range		**1.8**		**VDD**	
V_{IO}	SPI Rail Range		**1.8**		**VDD**	
I_{DD}	Supply Current, Conversion Mode	OUT[3:0] pins $R_L = \infty$			**4**	mA
PWR_{CONV}	Power Consumption, Conversion Mode	OUT[3:0] pins $R_L = \infty$			**21**	mW
I_{PD}	Supply Current, Power-Down Mode				**50**	µA
V_{POR}	Power-On Reset (*Note 8*)		**1.9**		**2.7**	V
AC ELECTRICAL CHARACTERISTICS						
t_{TRACK}	ADC Track Time	Dictated by SPI bus activity		**t_8+9×t_1**		µs
t_{HOLD}	ADC Hold Time	Dictated by SPI bus activity		**15×t_1**		µs
t_s	DAC Settling Time (*Note 9*)	25%FS to 75%FS code change, R_L = 2K, C_L = 200 pF			**20**	µs
t_{CONV}	Temperature Conversion Time				**25.85**	ms
SPI TIMING CHARACTERISTICS						
t_1	SPI Clock Period during ADC data access		**178**		**12500**	ns
t_1	SPI Clock Period during Temperature Sensor access		**178**		**5000**	ns
t_1	SPI Clock Period for all transactions not involving ADC or Temperature Sensor		**100**			ns
t_r	SCLK Rise Time				**2**	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_f	SCLK Fall Time				**2**	ns
t_2	SCLK HIGH Time		**8**			ns
t_3	SCLK LOW Time		**8**			ns
t_4	CSB set-up time to SCLK falling edge		**5**			ns
t_5	DIN Set-up time		**5**			ns
t_6	DIN Hold time		**4**			ns
t_7	CSB hold time after 24^{th} falling edge of SCLK		**10**			ns
t_8	CSB High Pulse Width		**30**			ns
t_{DH}	DOUT hold time after SCLK Rising Edge	C_L=30pF, VIO=1.8	**10**			ns
		C_L=30pF, 3V≤VIO≤5.25V	**5**			
t_{DD}	DOUT Delay after SCLK Rising Edge	C_L=30pF			**40**	ns
t_{11}	SCLK Delay after CSB Rising Edge		**3**			ns
t_{DOZ}	CSB Rising Edge to DOUT TRI-STATE			4	**10**	ns
t_{ZDO}	CSB Falling Edge to DOUT active	sink/source 200uA, C_L=150pF	**5**		**14**	ns

Note 1: “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: All voltages are measured with respect to GND = 0V, unless otherwise specified.

Note 3: When the input voltage (VIN) at any pin exceeds power supplies (VIN < GND or VIN > VDD), the current at that pin must not exceed 5mA, and the voltage (VIN) at that pin relative to any other pin must not exceed 6.0V. See Pin Descriptions for additional details of input circuit structures.

Note 4: The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 1.5k resistor into each pin. The Machine Model (MM) is a 200 pF capacitor charged to specified voltage then discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction process and then abruptly touches a grounded object or surface.

Note 5: Indicates the typical internal short circuit current limit. Sustained operation at this level will lead to device damage.

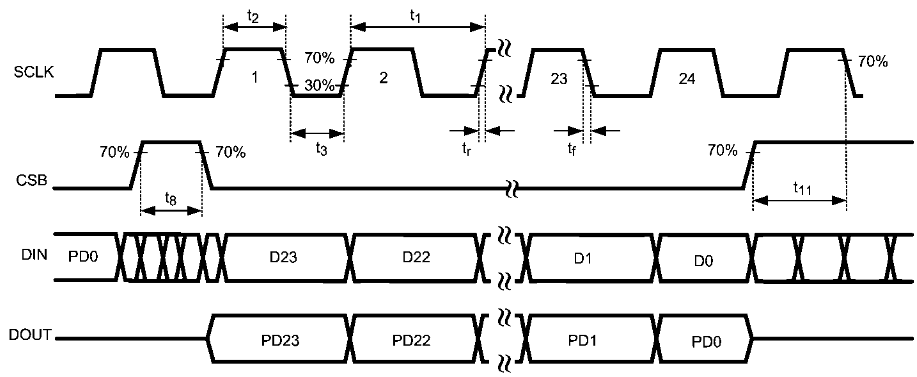
Note 6: DAC Offset is the y-intercept of the straight line defined by DAC output at code 0d12 and 0d1011points of the measured transfer characteristic.

Note 7: DAC Gain Error is the difference in slope of the straight line defined by DAC output at code 0d12 and 0d1011 points of transfer characteristic, and that of the ideal characteristic.

Note 8: During the power up the supply rail must ramp up beyond V_{POR} MIN for the device to acquire default state. After the supply rail has reached the nominal level, the rail can drop as low as V_{POR} MAX for the current state to be maintained.

Note 9: Device Specification is guaranteed by characterization and is not tested in production.

13.0 SPI Interface Timing Diagram



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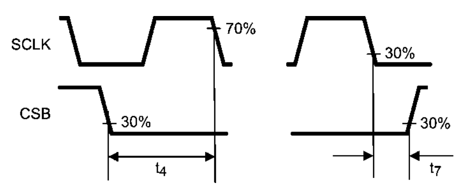

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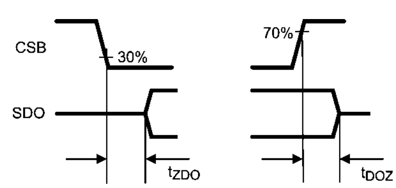

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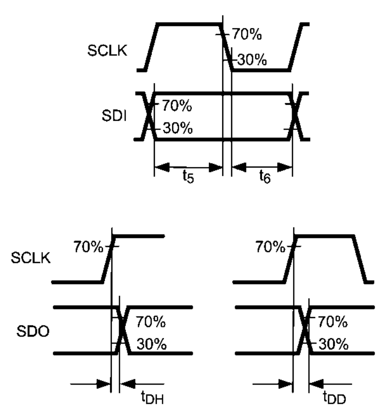

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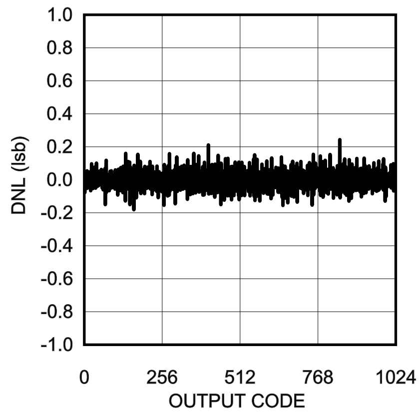
14.0 Typical Performance Characteristics

ADC: DNL



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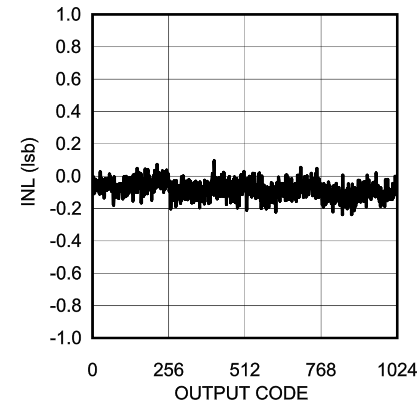
ADC: INL



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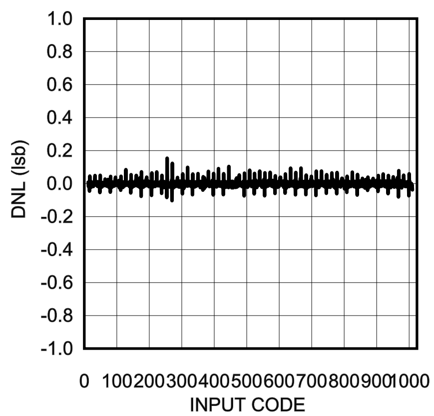
DAC: DNL



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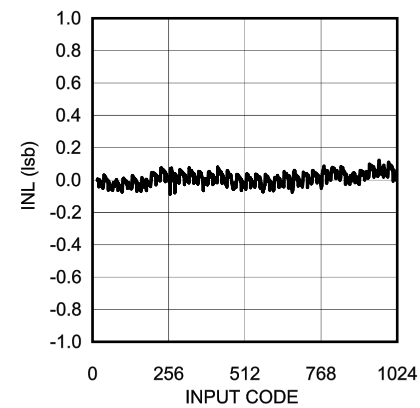
DAC: INL



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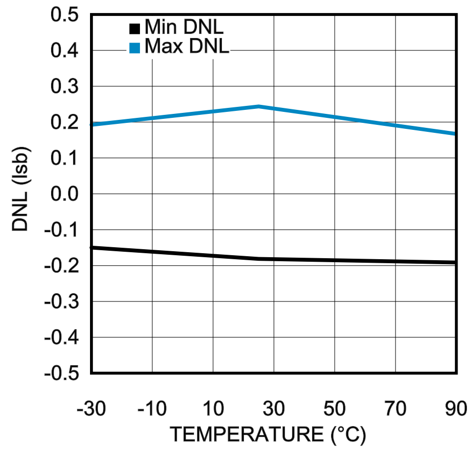
ADC: DNL vs. Temperature



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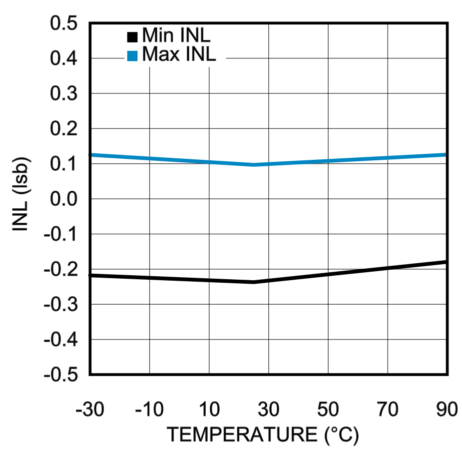
ADC: INL vs. Temperature



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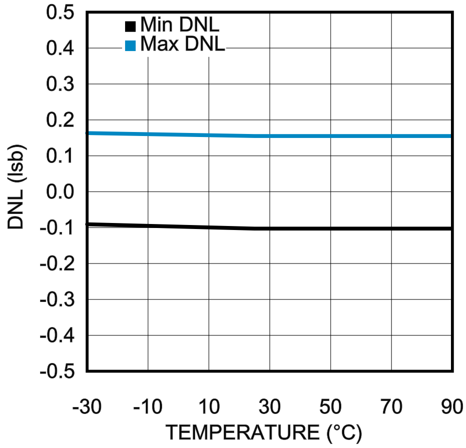
DAC: DNL vs Temperature



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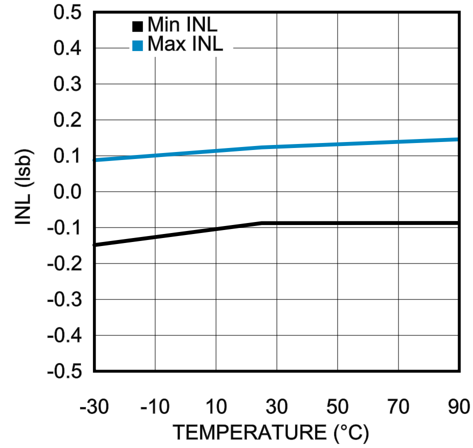
DAC: INL vs Temperature



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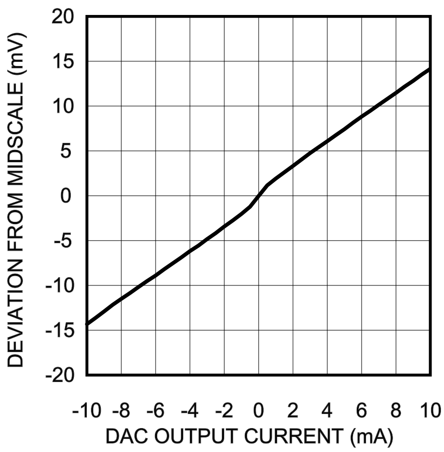
OUTx Output Load Regulation



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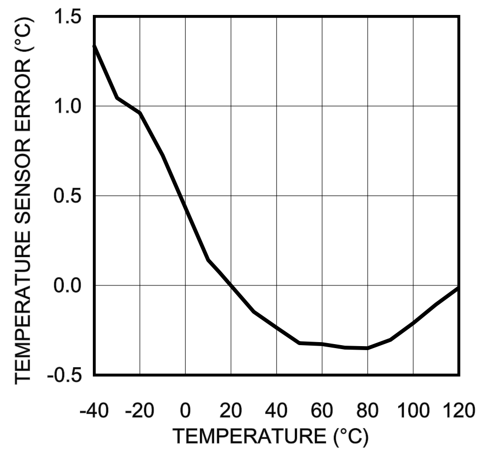
Temperature Sensor Error



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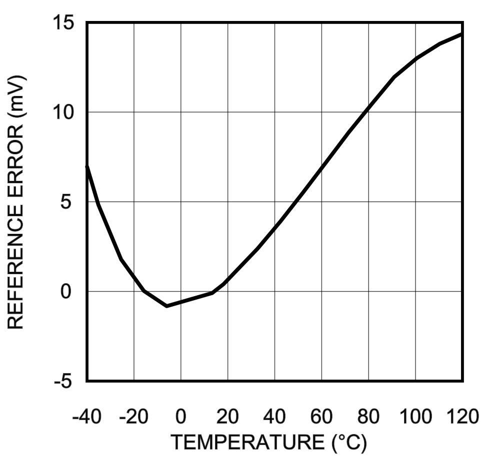
Internal Reference Output Temperature Drift



30152370

15.0 Instruction Set

The following is a complete listing of the instruction set supported by the LMP92018. Where applicable the default state or register content is indicated in **bold** type.

The digital interface (SPI) protocol is described in *Section 16.6 SERIAL INTERFACE*. The interface timing diagram is in *Section 13.0 SPI Interface Timing Diagram*

NOTE: the tables in following sections detail the data transfers of 2 subsequent SPI frames . The FRAME 1 column shows the user input into pin DIN of the device. The FRAME 2 column in the device output at DOUT.

15.1 TEMPERATURE SENSOR CONFIGURE

A single bit, TSS, controls the mode of operation of the internal temperature sensor. The bit can be set and tested via the SPI transactions shown in the following table. The internal temperature sensor is described in *Section 16.3 DIGITAL TEMPERATURE SENSOR*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:1**	**0**	**23**	**22:16**	**15:1**	**0**
READ	1	0010000	x	x	1	0010000	000000000000000	TSS
WRITE	0	0010000	000000000000000	TSS	0	0010000	000000000000000	0

x	Don't Care
TSS	1: Temperature Sensor in Continuous Conversion Mode **0: Temperature Sensor In One Shot Mode**

15.2 REFERENCE CONFIGURE

The internal reference mode of operation is controlled by a 3 bit sequence, CREF. The sequence can be set and tested via the SPI transactions shown in the following table. The reference block is described in *Section 16.4 INTERNAL VOLTAGE REFERENCE SOURCE*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:3**	**2:0**	**23**	**22:16**	**15:3**	**2:0**
READ	1	0010001	x	x	1	0010001	0000000000000	CREF
WRITE	0	0010001	0000000000000	CREF	0	0010001	0000000000000	000

x	Don't care
CREF	Reference Mode Selector **000: AREF external, DREF internal** 001: AREF and DREF internal; REF pin is internally disconnected 010: AREF and DREF external 011: AREF internal, DREF external 100: Deep Sleep 101: AREF and DREF internal; REF driven by internal reference 110: Deep Sleep 111: Deep Sleep

15.3 DAC CONFIGURE

The individual DACs can be enabled by setting a corresponding bit in the 4–bit CDAC word. The CDAC word can be set and tested via the SPI transactions shown in the following table. The DAC block is described in *Section 16.2 PROGRAMMABLE ANALOG OUTPUT SUBSYSTEM*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:4**	**3:0**	**23**	**22:16**	**15:4**	**3:0**
READ	1	0011000	x	x	1	0011000	000000000000	CDAC
WRITE	0	0011000	000000000000	CDAC	0	0011000	000000000000	0000

x	Don't care
CDAC	1: enables DAC corresponding to bit position **0: disables corresponding DAC** e.g. CDAC=[0101] enables DAC2 and DAC0

15.4 UPDATE ALL DACs

All 4 DAC channels' outputs can be simultaneously set to the same level corresponding to a 10–bit DDATA code. The sequence in the following table provides a WRITE only functionality. The DAC block is described in *Section 16.2 PROGRAMMABLE ANALOG OUTPUT SUBSYSTEM*.

	FRAME 1: DIN					FRAME 2: DOUT				
	Command		Payload			Command		Payload		
Bit→	**23**	**22:16**	**15:12**	**11:2**	**1:0**	**23**	**22:16**	**15:12**	**11:2**	**1:0**
WRITE	0	0011001	0000	DDATA	00	0	0011001	0000	0000000000	00

x	Don't care
DDATA	DDATA will be loaded into all all DACs' input registers simultaneously. DDATA is a 10–bit unsigned integer.

15.5 GENERAL CONFIGURATION

The device can indicate to the new ADC conversion data availability via the DRDYB pin. This functionality is enabled by setting the internal DRDY bit. The bit can be set and tested via the SPI transactions shown in the following table. Details of the DRDYB pin functionality are described in *Section 16.1.3 Conversion Sequence* and *Section 16.3 DIGITAL TEMPERATURE SENSOR*

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:1**	**0**	**23**	**22:16**	**15:1**	**0**
READ	1	0011110	x	x	1	0011110	000000000000000	DRDY
WRITE	0	0011110	000000000000000	DRDY	0	0011110	000000000000000	0

x	Don't Care
DRDY	1: Disables the DRDYB pin function **0: Enables the DRDYB pin function**

15.6 GPIO CONFIGURE

Individual bits of the general purpose digital I/O port can be configured to drive (output), or sense (input) only. Setting a corresponding bit in the 12–bit CGPIO word will enable that pin to drive. The sequences in the following table provide a READ and WRITE capability for the internal CGPIO register. The GPIO block is described in *Section 16.5 GENERAL PURPOSE DIGITAL I/O*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:12**	**11:0**	**23**	**22:16**	**15:12**	**11:0**
READ	1	0011111	x	x	1	0011111	0000	CGPIO
WRITE	0	0011111	0000	CGPIO	0	0011111	0000	000000000000

x	Don't Care
CGPIO	1: sets corresponding GPIO pin as output **0: sets corresponding GPIO pin as input** e.g. CGPIO=[000011110000] enables GPIO[7:4] pins as outputs, all other GPIO pins are inputs

15.7 STATUS

Internal bit, RDY, indicates when the device has completed its power-up sequence. The RDY bit can be tested via the SPI transaction shown in the following table.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:1**	**0**	**23**	**22:16**	**15:1**	**0**
READ	1	0100000	x	x	1	0100000	000000000000000	RDY

x	Don't Care
RDY	Internal Power On Reset circuit sets this bit **1: device ready** 0: device not ready

15.8 GPI STATE

The logic state present at the GPIO pins of the device is always reported in the SGPI register. The SGPI register contents can be tested via the SPI transaction shown in the following table. The GPIO block is described in *Section 16.5 GENERAL PURPOSE DIGITAL I/O*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:12**	**11:0**	**23**	**22:16**	**15:12**	**11:0**
READ	1	0110000	x	x	1	0110000	0000	SGPI

x	Don't Care
SGPI	Each bit Indicates the state at the corresponding GPIO pins of the device

15.9 GPO DATA

The GPIO pins configured to drive, will drive the state indicated in the CGPO register. The CGPO register can be set or tested via the SPI transactions shown in the following table. The GPIO block is described in *Section 16.5 GENERAL PURPOSE DIGITAL I/O*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		**Payload**		**Command**		**Payload**	
Bit→	**23**	**22:16**	**15:12**	**11:0**	**23**	**22:16**	**15:12**	**11:0**
READ	1	0110001	x	x	1	0110001	0000	CGPO
WRITE	0	0110001	0000	CGPO	0	0110001	0000	12'b0

x	Don't Care
CGPO	Each bit will be forced at the corresponding GPIO pin of the device. Bits corresponding to GPIO pins configured as inputs will be ignored. **CGPO[11:0]=0x000**

15.10 VENDOR ID

The 16–bit ID sequence is factory set, and can only be tested via the SPI transaction shown in the table below.

	FRAME 1: DIN			FRAME 2: DOUT		
	Command		**Payload**	**Command**		**Payload**
Bit→	**23**	**22:16**	**15:0**	**23**	**22:16**	**15:0**
READ	1	1000000	x	1	1000000	ID

x	Don't Care
ID	Vendor ID number. National Semiconductor **ID = 0x0028.**

15.11 VERSION/STEPPING

Version and Stepping words are factory set and can only be tested via the SPI transaction shown in the table below.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		**Payload**		**Command**		**Payload**	
Bit→	**23**	**22:16**	**15:4**	**3:0**	**23**	**22:16**	**15:4**	**3:0**
READ	1	1000001	x	x	1	1000001	VER	STEP

x	Don't Care
VER	Indicates the device version number. **VER=0x000**
STEP	Indicates stepping number. **STEP = 0x0**

15.12 DAC DATA REGISTER ACCESS

Each DAC's input data register, DDATA, is individually addressable, and its contents can be updated without affecting remaining 3 DACs. The content of each DDATA can be tested and set via the SPI transactions shown in the following table. The DAC block is described in *Section 16.2 PROGRAMMABLE ANALOG OUTPUT SUBSYSTEM*.

	FRAME 1: DIN						FRAME 2: DOUT					
	Command			Payload			Command			Payload		
Bit→	**23**	**22:18**	**17:16**	**15:12**	**11:2**	**1:0**	**23**	**22:18**	**17:16**	**15:12**	**11:2**	**1:0**
READ	1	10100	ADR	x	x	x	1	10100	ADR	0000	DDATA	00
WRITE	0	10100	ADR	0000	DDATA	00	0	10100	ADR	0000	10'b0	00

x	Don't Care
ADR	DAC address: 00: DAC0 01: DAC1 10: DAC2 11: DAC3
DDATA	DAC input data. DDATA is a 10–bit unsigned integer. **DDATA=0x000**

15.13 ADC INPUT MUX SELECT DATA READ COMMAND

The selection of the analog input, and the read-back of the ADC conversion result are completed by the SPI transaction shown in the following table. The ADC block is described in *Section 16.1 ANALOG SENSE SUBSYSTEM*.

	FRAME 1: DIN						FRAME 2: DOUT					
	Command			Payload			Command			Payload		
Bit→	**23**	**22:19**	**18:16**	**15:12**	**11:2**	**1:0**	**23**	**22:19**	**18:16**	**15:12**	**11:2**	**1:0**
READ	1	1100	ADR	x	x	x	1	1100	ADR	0000	ADATA	00

x	Don't Care
ADR	ADC Input Address: 000: IN0 001: IN1 010: IN2 011: IN3 100: IN4 101: IN5 110: IN6 111: IN7
ADATA	ADC output Data. ADATA is a 10–bit unsigned integer.

15.14 TEMPERATURE SENSOR OUTPUT REGISTER

The contents of the internal temperature sensor output register can be tested by the SPI transaction shown in the following table. The internal temperature sensor is described in *Section 16.3 DIGITAL TEMPERATURE SENSOR*.

	FRAME 1: DIN				FRAME 2: DOUT			
	Command		Payload		Command		Payload	
Bit→	**23**	**22:16**	**15:12**	**11:0**	**23**	**22:16**	**15:12**	**11:0**
READ	1	1110000	x	x	1	1110000	0000	TDATA

x	Don't Care
TDATA	Temperature Sensor Output Data. TDATA is a 12–bit signed integer.

15.15 NOOP — No Operation

NOOP offers no functionality of its own. It is provided as the means of completing the pending READ operation i.e. “pushing out” the data requested in the previous transaction.

	FRAME 1: DIN		FRAME 2: DOUT	
	Command	Payload	Command	Payload
Bit→	**23:16**	**15:0**	**23:16**	**15:0**
NOOP	00000000	x	00000000	16'b0

x	Don't Care

16.0 Functional Description

16.1 ANALOG SENSE SUBSYSTEM

The device is capable of monitoring up to 8 externally applied voltages. The system is centered around a 10-bit SAR ADC fronted by an 8-input mux.

16.1.1 Sampling and Conversion

The external voltage is sampled onto the internal C_{HOLD} capacitor during the TRACK period, see *Figure 1*. Once acquired, the stored charge is measured using the Successive Approximation Register (SAR) method. The timing of the internal state machine is governed by the user defined signals CSB and SCLK. The sequence of the events is described in *Section 16.1.3 Conversion Sequence*.

Attention should be paid to the output impedance of the sensed voltage source and the capacitance present at the INx input of the device (which is dominated by C_{HOLD} during TRACK time). The combined circuit's RC limits the bandwidth and settling time of the input signal. At maximum SPI bus data rate, it is recommended to limit the output resistance ROUT of the signal source to assure the accuracy of the conversion.

During the HOLD period (duration of t_{HOLD} specified in *Section 12.0 Electrical Characteristics*) , all mux switches are OFF, and the charge captured on C_{HOLD} is measured to produce an ADC output code. This charge is never lost during the conversion, unless the SCLK is so slow that the charge is lost due to the internal capacitor's leakage. Under normal conditions the charge stored is modified only during TRACK period.

Below is a typical ADC output code as a function of input voltage at device pin INx, x=0...7:

$$\text{ADATA} = \text{INT}\left(\frac{V_{INX}}{\text{AREF}} \times 1023\right)$$

In the expression above AREF is the reference voltage input to the internal ADC. See *Section 16.4 INTERNAL VOLTAGE REFERENCE SOURCE*.

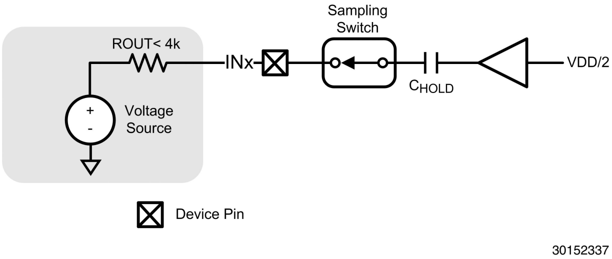


FIGURE 1. ADC During TRACK Period

16.1.2 Sampling Transient

As noted in *Section 16.1.1 Sampling and Conversion* the charge acquired during TRACK period is maintained throughout the conversion process. Since the successive sample operations will involve different input potentials an instantaneous current will flow at the beginning of TRACK period. This always leads to temporary disturbance of the input potential. This current, and resulting disturbance, will vary with the magnitude of the sampled signal and source impedance ROUT, see *Figure 1*. If ROUT is excessive, and resulting RC time constant of the input circuit too long, the preceding sample may affect the new sample's accuracy.

If high ROUT cannot be avoided, another method of improving the acquisitin accuracy is to lengthen the TRACK time. The ADC TRACK time is fully controlled by the user inputs CSB and SCLK, see *Figure 2*. The time allotted for the C_{HOLD} to settle can be arbitrarily adjusted via the length of the CSB=High period and the frequency of SCLK, subject to limitations on CSB and SCLK timing as shown in *Section 12.0 Electrical Characteristics* .

16.1.3 Conversion Sequence

The ADC conversion sequence and output activity are shown in *Figure 2*. The ADC readback occupies 2 SPI frames. The first frame is used to issue a read command and connect the ADC input to the specified device input pin INx. At the end of the first frame, at the rising edge of the CSB, the ADC sampling capacitor is connected to the signal source, INx, and the TRACK period begins. The second frame executes the SAR algorithm (the HOLD period) on the acquired sample and shifts the resulting data out through the DOUT output. The TRACK period extends for 9 SCLK cycles, then the mux disconnects the sampling capacitor from the signal source, and the SAR operation begins. The data is shifted out MSB first. Once the SAR operation is completed, the ADC powers down for the remainder of the second frame.

If DRDYB output pin functionality is enabled, see *Section 15.5 GENERAL CONFIGURATION*, then DRDYB output will be low while ADC output data is present at DOUT.

If the ADC is not in TRACK or HOLD, the internal PD (Power Down) signal of the ADC is asserted thus powering down all the active circuits of the ADC, and opening all analog input mux switches. See the PD period in the *Figure 2*.

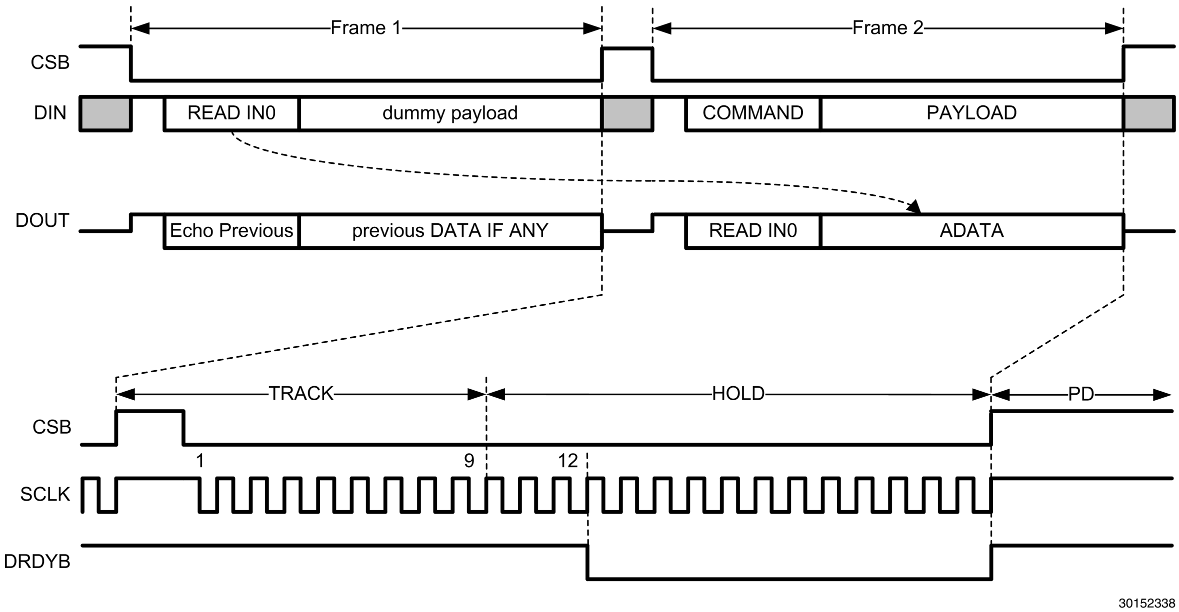


FIGURE 2. ADC Sequence Diagram

16.1.4 ADC Reference Selection

By default, the ADC operates from the external reference voltage applied at the REF pin of the device. It should be noted that due to the architecture of the ADC the DC current flowing into the REF input is zero during conversion. However, the transient currents (see I_{VREF} in *Section 12.0 Electrical Characteristics*) during the HOLD time can be significant. For further details of reference source selection see *Section 16.4 INTERNAL VOLTAGE REFERENCE SOURCE*

Selection of the ADC reference source automatically dictates the attenuation level of the input signal. *Figure 3* shows the ADC input configuration during the TRACK period when the REF pin is chosen as the source of the reference voltage. The entire C_{HOLD} available is used to acquire the signal. The transfer function of the ADC in this configuration remains as shown in *Section 16.1.1 Sampling and Conversion*

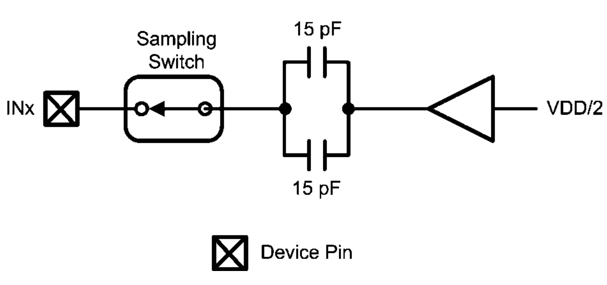


FIGURE 3. ADC Sampling when AREF is Externally Supplied

In contrast, the *Figure 4* shows the sampling capacitor during TRACK period when the internally generated reference is selected as the reference source of the ADC. In this configuration ½C_{HOLD} is used to sample the input signal effectively attenuating it by a factor of 2. The resulting overall ADC transfer function becomes:

$$ADATA = INT\left(\frac{V_{INX}}{2 \times AREF} \times 1023\right)$$

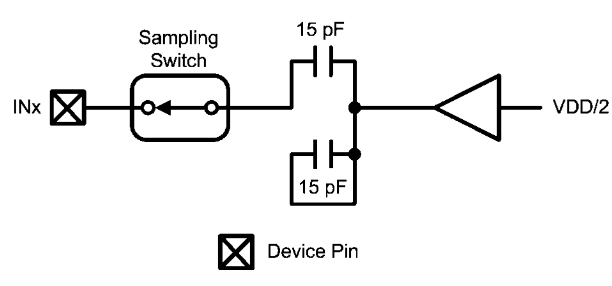


FIGURE 4. ADC Sampling when AREF is Internally Supplied

16.2 PROGRAMMABLE ANALOG OUTPUT SUBSYSTEM

This subsystem consists of 4 identical DACs whose output is a function of the user programmable registers DACx. This functionality is described in *Section 16.2.1 DAC Core*. The DAC input registers are individually addressable, as described *Section 15.12 DAC DATA REGISTER ACCESS*. The user can also update all of the DAC input registers to the same value with a single SPI command. See *Section 15.4 UPDATE ALL DACs*

Each DAC channel can be individually enabled/disabled via the SPI interface command. See *Section 15.3 DAC CONFIGURE*. When a channel is disabled, its output OUTx is in HiZ state, but the DAC input register still maintains its data.

User can select the source of the reference input to all DACs. This functionality is described in *Section 16.2.2 DAC Reference Selection*

16.2.1 DAC Core

The DAC core is based on a Resistive String architecture which guarantees monotonicity of its transfer function. The input data is single-registered, meaning that the OUTx of the DAC is updated as soon as the data is updated in the DAC input data register at the end of the SPI transaction.

The functional diagram of the DAC Core is shown in *Figure 5*

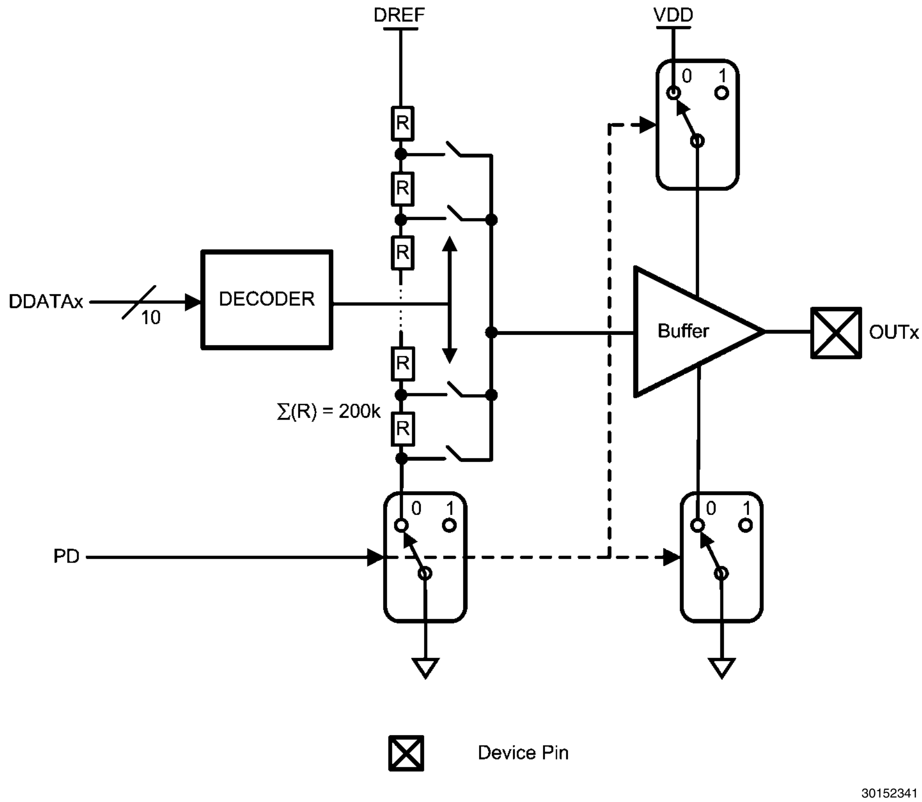


FIGURE 5. DAC Block Diagram

The ideal DAC core transfer function from DATAx to OUTx , x=0...3, can be expressed as:

$$OUTx = DREF\left(\frac{DDATAx}{1024}\right)$$

The above expression is subject to non-idealities of the resistor string and limitations of the output buffer. These limitations are tabulated in *Section 12.0 Electrical Characteristics*

In *Figure 5*, the PD (Power Down) signal is asserted when the given channel is disabled via the SPI command. The PD causes the DAC buffer bias currents to shut down, and it breaks the current path through the resistive string.

16.2.2 DAC Reference Selection

All DAC channels operate from the same, user selectable, reference source. In *Figure 5*, DREF input can be supplied by the external source, applied to the REF pin of the device, or from the internal reference generator block. The reference block functionality is described in *Section 16.4 INTERNAL VOLTAGE REFERENCE SOURCE*.

Reference selection automatically forces configuration of the DACs' output buffers. If the external reference source, which is DREF driven by the REF device pin, is selected then all of the DAC output buffers are in 1x configuration, as seen in*Figure 6*. In the external reference mode, each active DAC presents a resistive load to the source attached to the device's REF pin, see *Figure 5* and *Figure 9*.

The overall DAC transfers function remains as shown in *Section 16.2.1 DAC Core*

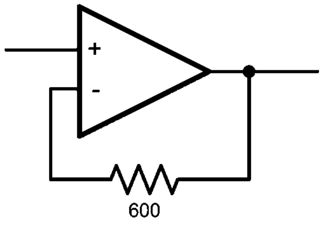


FIGURE 6. DAC Buffer when DREF Externally Supplied

If the internal reference generator is selected to drive the DAC's DREF input, then all of the DACs' buffers are automatically forced into 2x gain configuration as shown in *Figure 7*. This results in an overall transfer function of the DACs to change to:

$$\text{OUTx} = 2 \times \text{DREF}\left(\frac{\text{DDATAx}}{1024}\right)$$

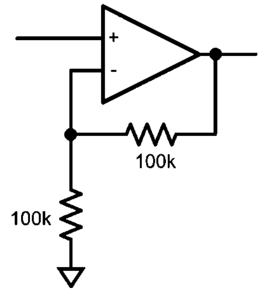


FIGURE 7. DAC Buffer when DREF Internally Supplied

16.3 DIGITAL TEMPERATURE SENSOR

The local temperature sensor (TS) operates in one of the 2 possible modes: Continuous or One-Shot. The user selects the mode of operation via the SPI instruction, see *Section 15.1 TEMPERATURE SENSOR CONFIGURE*. The output of the temperature sensor is a 12 bit signed integer, where each LSB represents 0.0625°C. Temperature sensor's output code (TDATA) examples are shown in *Table 1*.

TABLE 1. Temperature Readout Examples

Temperature	TDATA
125°C	0111.1101.0000
25°C	0001.1001.0000
0.0625°C	0000.0000.0001
0°C	0000.0000.0000
–0.0625°C	1111.1111.1111
–40°C	1101.1000.0000

In Continuous mode, the temperature sensor operates in the background and independently of the SPI bus activity. Subsequent temperature conversion results are stored in the output register which can be accessed by the user via the SPI interface.

In One-Shot mode temperature sensor is inactive until the user issues an instruction, via SPI interface, to read the temperature sensor data. The temperature conversion commences at the rising edge of CSB following the read instruction. After the delay of t_{CONV}, the new temperature data is available in the temperature sensor output register. If configured, the DRDYB output indicates when the temperature conversion has been completed, see .

The SPI instruction for accessing the temperature data is described in *Section 15.14 TEMPERATURE SENSOR OUTPUT REGISTER*

In *Figure 8* below a One-Shot temperature read transaction is shown. The temperature readback occupies 2 SPI frames: the first frame is used to issue temperature sensor read instruction, the second frame is used for the data readback. The falling edge of the DRDYB signal indicates the instance the new temperature data is present in the output register. The DRDYB is deasserted by the rising edge of the CSB.

NOTE: The DRDYB output in One-Shot temperature conversion mode is asynchronous to the SCLK of the SPI interface. DRDYB functionality is not provided in the Continuous mode of the temperature sensor operation.

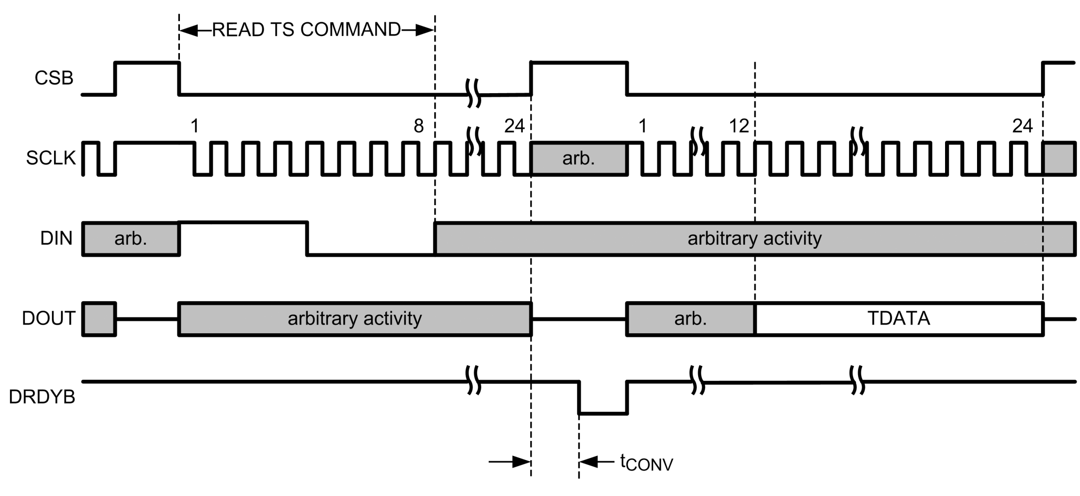


FIGURE 8. One-Shot Temperature Read Sequence

16.4 INTERNAL VOLTAGE REFERENCE SOURCE

The device has a built in precision 2.5V reference block which can be used to provide reference potential to either the ADC (AREF) or the DACs (DREF), both at once, or to external load via REF pin. The precision reference is always isolated from its loads by individual buffers, see *Figure 9*.

The CREF register sets the reference block mode of operation. The SPI instruction to update or read contents of the CREF register is shown in *Section 15.2 REFERENCE CONFIGURE*. The switch activity due to the CREF content is tabulated in *Table 2*.

The modes corresponding to CREF=(100) or (110) or (111) are the Deep Sleep modes. In these modes the internal temperature sensor, the ADC, the DACs, and the reference block buffers (but not the 2.5V reference) are powered down.

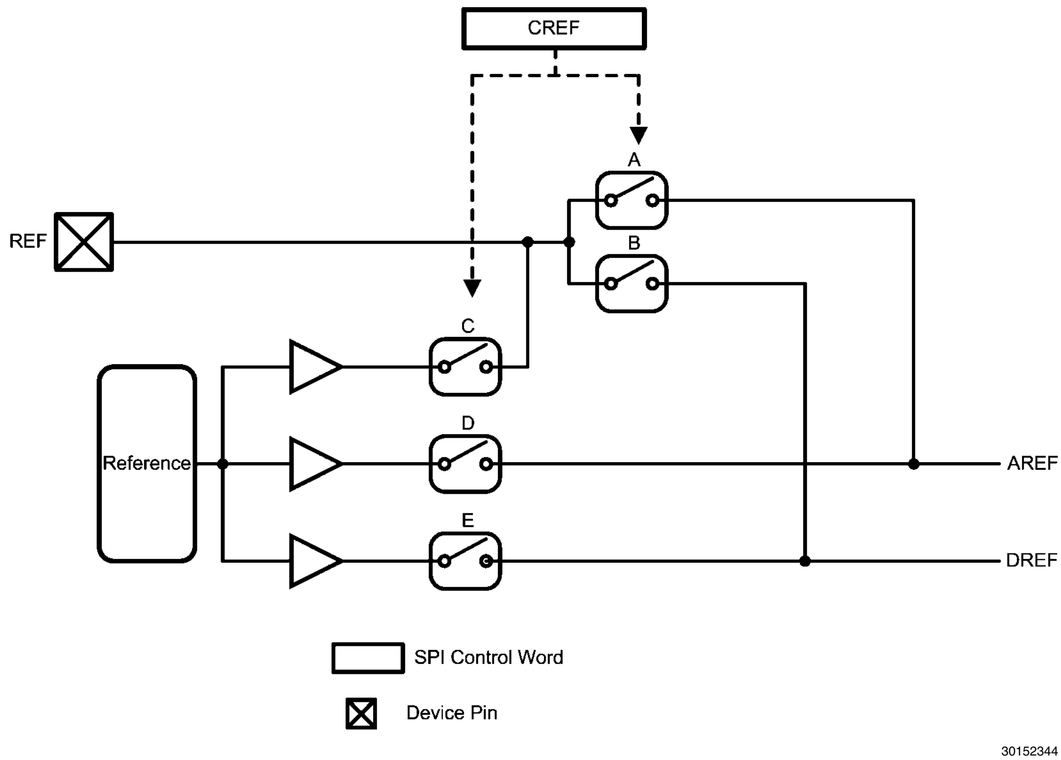


FIGURE 9. Reference Selector Diagram

TABLE 2. Reference Selector Functionality (1 to CLOSE Switch)

	Switch				
CREF	**A**	**B**	**C**	**D**	**E**
000	1	0	0	0	1
001	0	0	0	1	1
010	1	1	0	0	0
011	0	1	0	1	0
100	0	0	0	0	0
101	0	0	1	1	1
110	0	0	0	0	0
111	0	0	0	0	0

16.5 GENERAL PURPOSE DIGITAL I/O

The GPIO[11:0] port is memory mapped to registers SGPI and CGPO. Both registers are accessible through the SPI interface.

The SGPI register content reflects at all times the digital state at the GPIOx device pins. The format of the read command of the General Purpose Digital I/O is shown in *Section 15.8 GPI STATE*.

The GPIOx pins can be configured as outputs by setting the individual bits in the CGPIO registers. Each bit in CGPIO register enables corresponding output buffer in the GPIOx port. See *Section 15.6 GPIO CONFIGURE*. Once the drive is enabled, the logic state at the outputs is dictated by the contents of the CGPO register. See *Section 15.9 GPO DATA*.

The functional diagram of the General Purpose Digital I/O is shown in *Figure 10*.

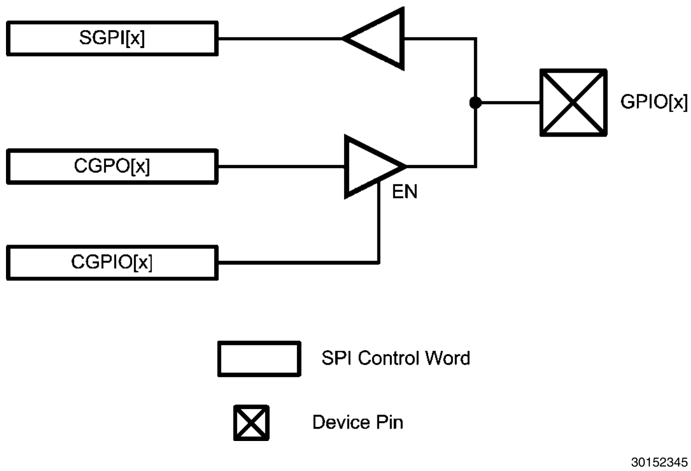


FIGURE 10. General Purpose Digital I/O Diagram

16.6 SERIAL INTERFACE

The 4-wire interface is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the *Section 13.0 SPI Interface Timing Diagram* for timing information of the read and write sequences. The serial interface uses four signals CSB, SCLK, DIN and DOUT.

A bus transaction is initiated by the falling edge of the CSB. Once CSB is low, the input data is sampled at the DIN pin by the falling edge of the SCLK, and shifted into the internal shift register (FIFO). The output data is put out on the DOUT pin on the rising edge of SCLK. At least 24 SCLK cycles are required for a valid transfer to occur. If CSB is raised before 24th rising edge of the SCLK, the transfer is aborted and preceding data ignored. If the CSB is held low after the 24th falling edge of the SCLK, the data will continue to flow through the internal shift register (FIFO) and out the DOUT pin. When CSB transitions high, the internal controller decodes the FIFO contents — most recent 24 bits that were received before the rising edge of CSB.

While CSB is high, DOUT is in a high-Z state. At the falling edge of CSB, DOUT presents the MSB of the data present in the shift register. DOUT is updated on every subsequent falling edge of SCLK (note — the first DOUT transition will happen on the first rising edge AFTER the first falling edge of SCLK when CSB is low).

The 24 bits of data contained in the FIFO are interpreted as an 8 bit COMMAND word followed by 16 bits of DATA. The general format of the 24 bit data stream is shown in *Figure 11*. The full Instruction Set is tabulated in *Section 15.0 Instruction Set*.

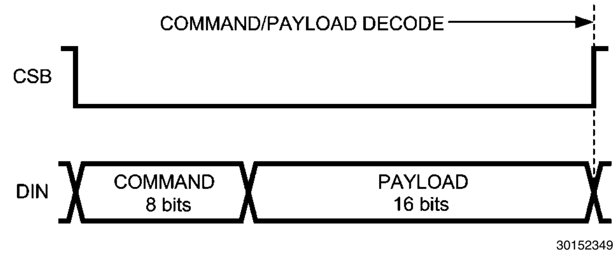


FIGURE 11. General SPI Frame Format

16.6.1 SPI Write

SPI write operation occupies a single 24–bit frame, as shown in *Figure 12*. Write operation always starts with a leading 0 (zero) in the 8–bit COMMAND sequence. The format of the data transfer and user instruction set is shown in *Section 15.0 Instruction Set*.

Note that write operation also produces DOUT activity. The DOUT output echoes back the previous frame's COMMAND byte, followed by 16 zeros.

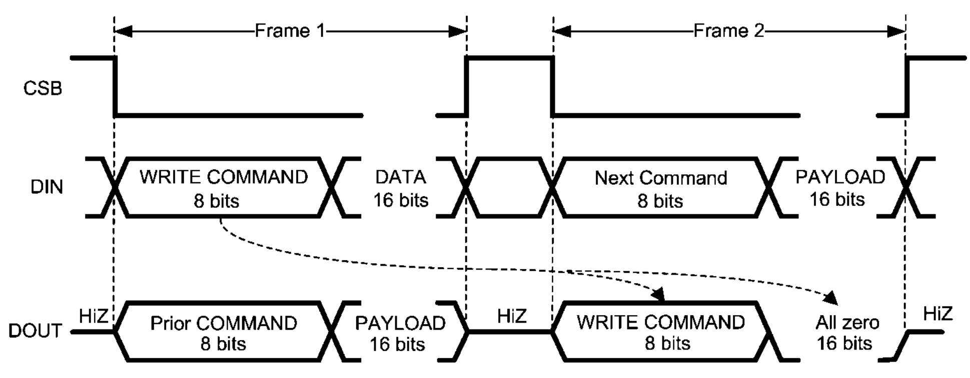


FIGURE 12. SPI Write Transaction

16.6.2 SPI Read

The read operation requires all 4 wires of the SPI interface: SCLK, CSB, DIN, DOUT. The simplest read operation occurs automatically during any valid transaction on the SPI bus since DOUT pin always shifts out the leading 8 bits (COMMAND) of the previous transaction — this is regardless of the RW bit setting in the COMMAND byte. This functionality gives the user an easy method of verifying the SPI link.

Reading of the specific content requires 2 SPI frames, as shown in *Figure 13*. The first frame is used to issue a read command, which always begins with RW bit set in the COMMAND byte. The second frame echoes back the first frame's COMMAND byte, followed by the 16–bit PAYLOAD containing the requested data. Consult *Section 15.0 Instruction Set* for the COMMAND format and returned data alignment within PAYLOAD.

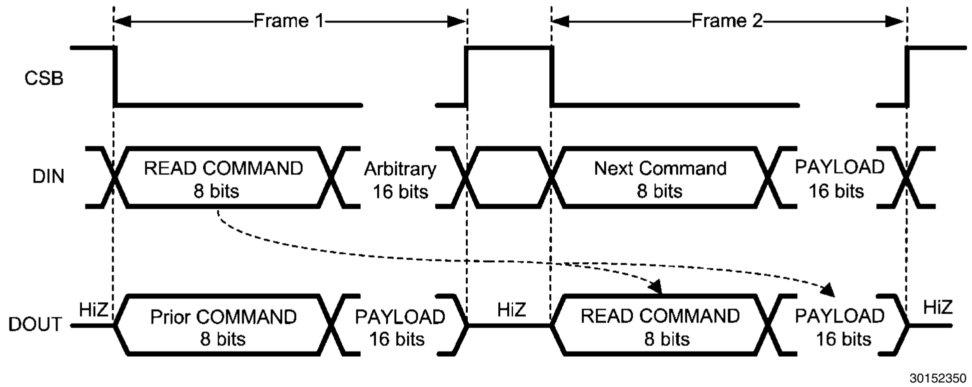


FIGURE 13. SPI Read Transaction

16.6.3 SPI Daisy Chain

It is possible to control multiple LMP92018s with a single master equipped with one SPI interface. This is accomplished by connecting the multiple LMP92018 devices in a Daisy Chain. The scheme is depicted in *Figure 14*. A chain of arbitrary length can be constructed since individual devices do not count the data bits shifted in. Instead, they wait to decode the contents of their respective shift registers until CSB is raised high.

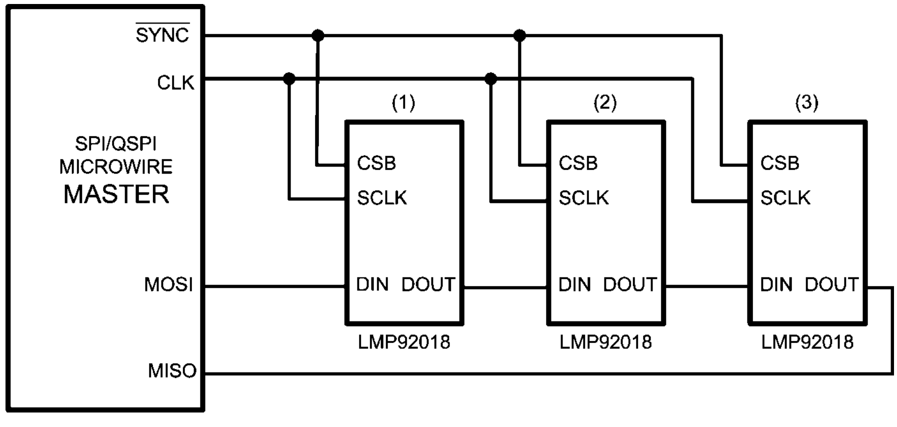


FIGURE 14. SPI Daisy Chain

A typical bus cycle for this scheme is initiated by the falling CSB. After the 24 SCLK cycles new data starts to appear at the DOUT pin of the first device in the chain, and starts shifting into the second device. After the 72 SCLK cycles following the falling CSB edge, all three devices in this example will contain new data in their input shift registers. Raising CSB will begin the process of decoding data in each device. When in the Daisy Chain the full READ and WRITE capability of every device is maintained.

A sample of SPI data transfer appropriate for a 3 device Daisy Chain is shown in *Figure 15*.

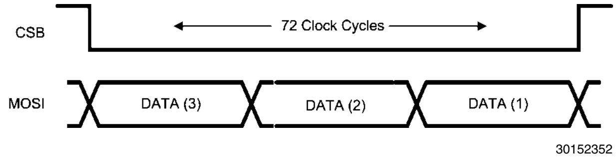
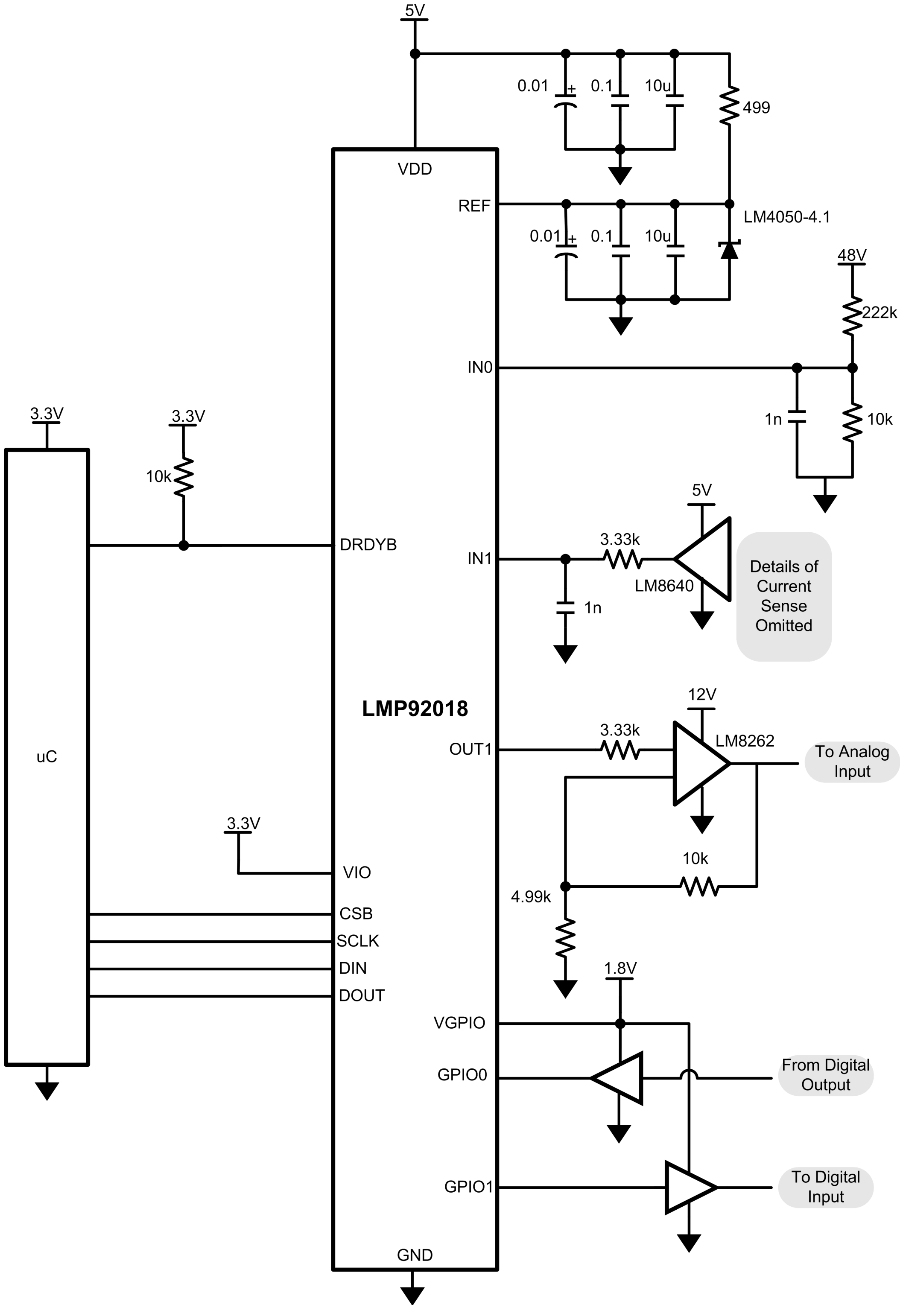
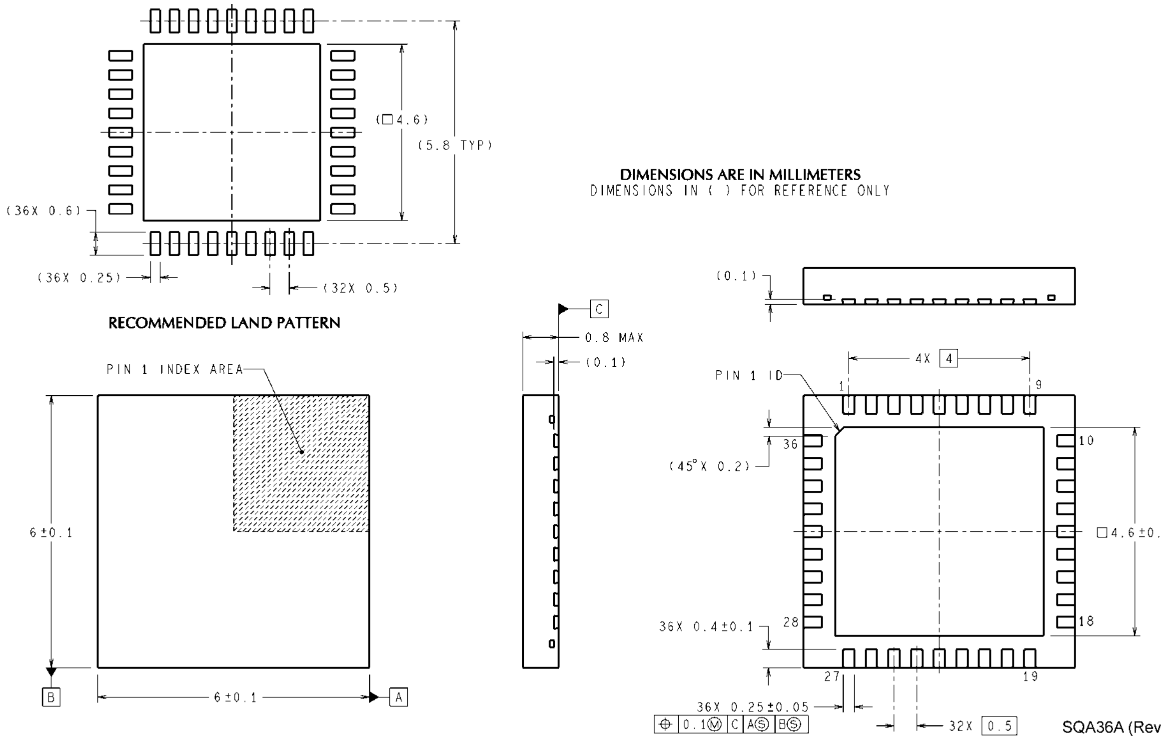


FIGURE 15. SPI Daisy Chain Transaction

17.0 Application Circuit Example



18.0 Physical Dimensions inches (millimeters) unless otherwise noted



SQA36A (Rev A)

LLP-36 Package
NS Package Number SQA36A

Notes

Notes

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